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Special Type of Circuit Dual Hypergraph

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ABSTRACT

In this paper, floorplanning with L-shaped modules and partitioning of a special type of circuit dual hypergraph has been focused. Two theorems have been established related to this type of VLSI circuits and short circuit testing.

Keywords: *Circuit dual hypergraph, VLSI floorplan, L-shaped floorplan, short-circuit testing, graph coloring, line of sight graph.*

I. INTRODUCTION

It has been found that VLSI design is an important part of CAD technology of Computer Science and Engineering, Electronics and Telecommunication and Electrical Engineering. There are many unsolved problems related to applications of Graph in this field. Few works have been studied for VLSI design technology by Kalita B [1, 2], Y. Lai and S. M. Leinwand [3], S. M. Sait and H. Youssef [4], Sadiq M. Sait and Habib Youssef [5], D.F. Wong and C.L. Liu [6], Yachyang Sun and C. L. Liu [7], W. R. Heller et al [8].

Circuit dual hypergraph is the hypergraph that can be obtained from a circuit placing modules as the vertices of the hypergraph and the links among them is represented by the edges of the hypergraph [14]. Floorplanning is a major step in the VLSI circuits design. Many authors Sadiq M. Sait and Habib Youssef [5], W. R. Heller et al [8], K. Maling and et al[9], R. H. J. M. Otten[10], D. P. LaPotin and S. W. Director [11], B. Preas and C. S. Chow[12], L. S. Woo, C. K. Wong, and D. T. Tang[13] have been discussed various results related to floorplanning design. A good layout is one which occupies minimum area, uses short wires for interconnection and as few vias as possible [5]. Layout design is complicated by different constraints. The possible constraints may be minimize area, minimize wire length, minimize delays etc. There are different methods using for floorplanning [5].

It is also discussed that traditional graph theoretical methods and algorithms can be applied to the floorplanning problems. A graph theoretic rectangular dualization method may be used to construct rectangular floorplanning [3]. The rectangular dualization problem is transformed into a matching problem on bipartite graphs. Therefore, rectangular dualization is used to Floor-planning design [4].

The inclusion of L-shaped regions in a floorplan provides additional flexibility in achieving the goal of minimizing the total area of a floorplan [6]. The concept of graph coloring can be used in circuit partitioning and also to study the number of short circuit tests need to execute [14].

Thickness and crossing of non-planar graph holds a special place in VLSI physical design. The lower bound of crossing of complete graph has been found by Kalita [1]. A non-planar graph K(2m+2, $2m^2$+3m) for m≥2 has been considered with two vertices of degree 2m and all other vertices are of degree 2m+1. It has been proved that this graph is Hamiltonian and it has edge disjoined Hamiltonian circuits [1]. It has been stated that the lower bound of crossing can be evaluated as $M(K_{2m+2}) - L(K_{2m+2}) = 2n+1$ for $n \geq 0$ with simultaneous changes of $m \geq 2$ [1] where $M(K_{2m+2})$ is the upper bound and $L(K_{2m+2})$ is the lower bound of crossings of the complete graph $K_{2m+2 \text{ for } m \geq 2}$. This type of graphs can be obtained from the circuits as shown in Fig. 1 [1].

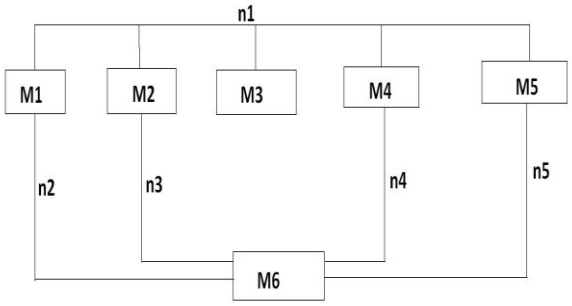

Fig. 1 Circuit of 6 modules and 5 nets

These kinds of graphs are always there in the circuits having 2n+3 numbers of nets for $n \geq 1$ with simultaneous changes of m≥2 [1]. Further, Katila[1] has stated and proved theorems for special type of hypergraphs such as 1-uniform, 2-uniform, 3-uniform etc. An algorithm has been given to convert a hypergraph of vertices 2m+2 for m≥2 to a graph [1]. A special planar graph G(2m+2, 6m) can be obtained from the complete graph K_{2m+2} for m≥2 [1]. This graph is subgraph of graph K(2m+2, $2m^2$+3m) [1]. It has also been stated that graph G(2m+2, 6m) will give rectangular floorplan without overlap [1].

The circuit having the graph G(2m+2, 6m) will contain four partitions and possible sort circuit tests will be six [2]. If the weight of the vertices is unity, then this circuit graph will have r partitions where $2 \leq r \leq 2m+1$ for $m \geq 2$ [2]. Again if the weight of the vertices is two and one partition contains two vertices and other contains 2n+2 vertices for $n \geq 1$, then r will be equals to two (r=2) [2]. Also if weight of the vertices is three and one partition contains one vertex and other contains 2n+3 vertices for n

≥ 1 with simultaneous changes of m ≥ 2, then r will be equals to two (r=2) [2].

Area minimization problem for floorplans of VLSI circuit design with only rectangular regions is an NP-complete problem [6]. So, we tried to find a pattern that shall have L-shaped rectangular modules to avoid NP-complete problem. The new structure of a circuit dual hypergraph has been found [2].

In this paper, we present theoretical explanation for that special circuit dual hypergraph of a VLSI circuit.

II. THEOREM 1

Let K (2m+2, 6m) for m≥2 be a circuit dual hypergraph where 2m+2 for m ≥ 2 represents the number of modules in the chip. If the degrees of modules are between 4 to 2m, and then this circuit dual hypergraph gives floorplan with L-shaped regions.

A. Proof 1

Let K (2m+2, 6m) be a circuit dual hypergraph for m≥2 having 2m+2 number of modules. Now, suppose m = 2 then, the number of modules is (2m+2 = 6) six and the number of edges is (6m = 12) twelve. So, we draw the circuit graph (Fig. 2) with degrees of the vertices between 4 and 2m for this graph and the possible floorplan (Fig. 3) for it which definitely contains L-shaped modules.

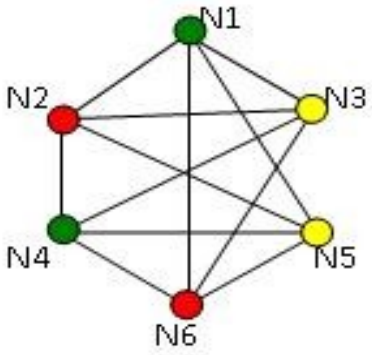

Fig. 2 Circuit graph of K (6, 12) i.e. m=2

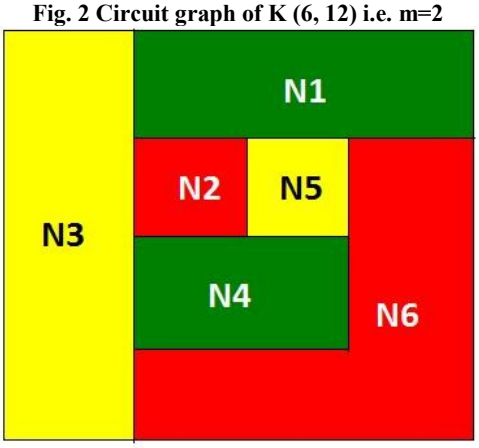

Fig. 3 Possible floorplan of the circuit graph in Fig. 2

Next, we suppose m = 3 then the number of modules is (2m+2 = 2 * 3 + 2 = 8) eight and the number of edges is (6m = 6 * 3 = 18) eighteen. Restricting the degree of vertices between 4 and 2m, we draw the circuit graph (Fig. 4) and floorplan (Fig. 5) for it.

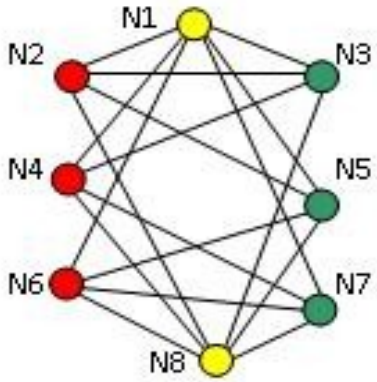

Fig. 4 Circuit graph of K (8, 18) i.e. m=3

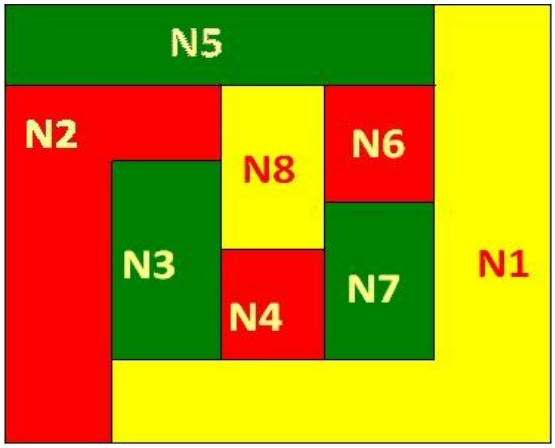

Fig. 5 Possible floorplan of the circuit graph in Fig. 4

Since this result is true for m = 2 and m = 3 that is we have floorplan with L-shaped modules, so we assume that the result will be true for m = k. For m = k, the number of modules will be 2k+2 and the number of edges will be 6k. We have seen that the numbers of modules are always even and as well as the numbers of edges. Hence, we can say that 2k+2+2 and 6k+6 are also even. Therefore, 2k+2+2 = 2(k+1) + 2 is even and 6k+6 = 6(k+1) is also even.

So, using Mathematical Induction method, we prove that this special circuit dual hypergraph K(2m+2, 6m) for m≥2 having 2m+2 number of even modules and 6m number of even edges always represents same kind of circuit graph and floorplan.

It is clear that this type of floorplan is always gives L-shaped regions. The inclusion of L-shaped regions in a floorplan provides additional flexibility in achieving the goal of minimizing the total area of a floorplan [6]. Area minimization problem for floorplans with only rectangular regions is an NP-complete problem **[6]**.

III. THEOREM 2

The circuit of this hypergraph always needs three partitions and hence three tests for short-circuit.

A. Proof 2

From the figures 2 and figures 4, we also show that the line of sight graph of this type circuit shall have three colors if the degrees of vertices are between 4 and 2m. So, the circuits of this hypergraph shall have three partitions and it needs three short-circuit tests since ${}^{3}C_{2} = 3$.

IV. RESULTS

Apart from mathematical induction, we find the following table (Table 1) to support the work.

TABLE I
RESULTS FOR DIFFERENT VALUES OF 'M'

m	No. of modules (2m+2)	No. of edges (6m)	Weight of the modules ($4 \leq$ weight $\leq$ 2m)	No. of colors (N)	No. of short circuit (${}^{N}C_{2}$)
2	6	12	4	3	3
3	8	18	6	3	3
4	10	24	8	3	3
5	12	30	12	3	3
6	14	36	14	3	3
7	16	42	16	3	3
8	18	48	18	3	3

We also draw the circuit dual hypergraphs which is also the line of sight graphs and floorplans for the following values of 'm' which also support both the theorems.

For m = 4, then K (10, 24) [Fig. 6, Fig. 7]

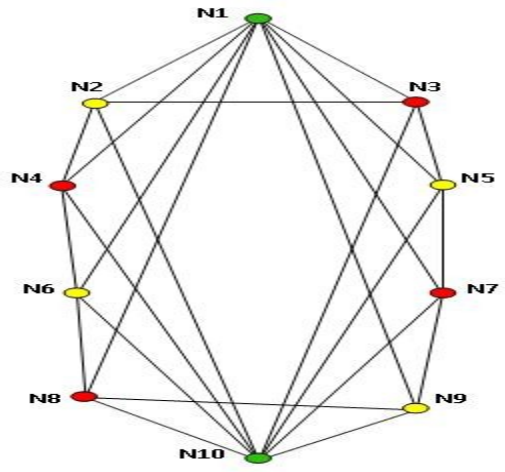

Fig. 6 Circuit graph of K (10, 24) i.e. m=4

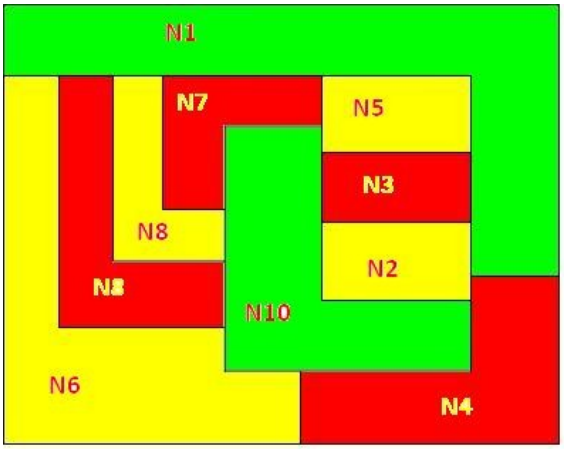

Fig 7: Possible floorplan of the circuit graph in Fig. 6

For m = 5, then K (12, 30) [Fig. 8, Fig. 9]

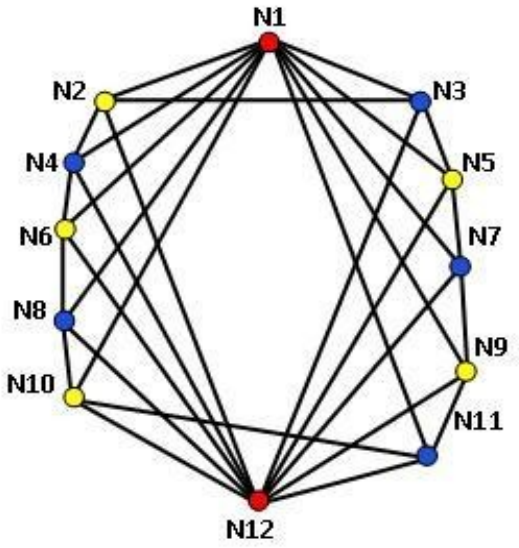

Fig. 8 Circuit graph of K (12, 30) i.e. m=5

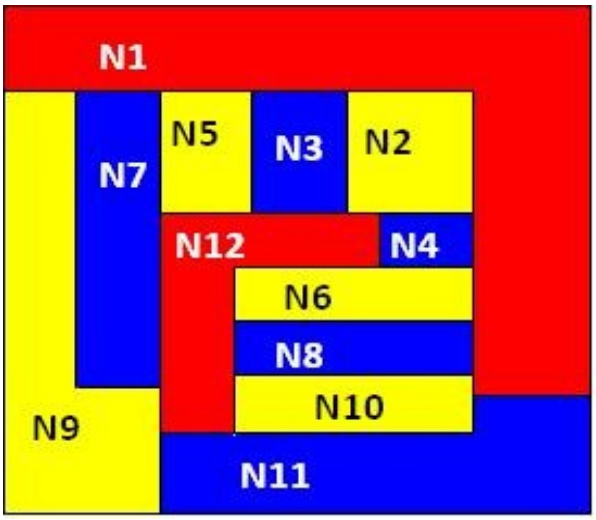

Fig 9: Possible floorplan of the circuit graph in Fig. 8

For m = 6, then K (14, 36) [Fig. 10, Fig. 11]

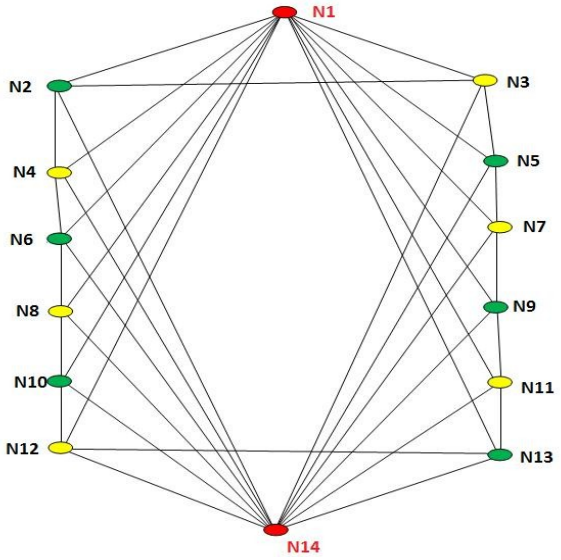

Fig 10: Circuit graph of K (14, 36) i.e. m=6

Fig 11: Possible floorplan of the circuit graph in Fig. 10

V. CONCLUDING REMARKS

We have presented in this paper only two theorems for a special type of circuit dual hypergraph. The second theorem is derivation of the first one. Both theorems are derived using mathematical induction method and completely theoretical. If any circuit dual hypergraph falls under this category, then according to our theorem, those circuits shall have only three partitions, need three tests for short circuit and the floorplan shall contain L-shaped modules.

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